ADV MATH SCI JOURNAL
Advances in Mathematics: Scientific Journal **9** (2020), no.6, 3581–3592
ISSN: 1857-8365 (printed); 1857-8438 (electronic)
https://doi.org/10.37418/amsj.9.6.36 Spec. Issue on RDESTM-2020

SWITCHING POWER OF CNFET BASED 6-TRANSISTOR 1-BIT FAST ADDER IMPLEMENTED USING CADENCE

MD. ZUBAIR ALAM EMON[1], PROVAT CHANDRA PAUL, NABILA MAYEEN, NUSRAT ALAM, AND MD. IQBAL BAHAR CHOWDHURY

ABSTRACT. This paper presents a simple design of a 1-bit pass transistor logic based 'Fast Adder' module implemented using carbon nanotube field-effect transistors (CNFETs). 'Sum' and 'carry' outputs of the fast adder circuit has been generated using the XOR function and hence, the module uses only 6 transistors. This Fast adder module is implemented in Cadence with 32 nm CNFET technology with 0.9 V as supply. The switching power of this adder has been observed at different states through the simulations using Cadence at 100 MHz input frequency. 0.8 nW is found to be the average switching power in case of no load. Although there is degradation in the outputs for one/two states owing to circuit behavior and CNFET properties, the implemented fast adder is more cost-effective than the conventional adders.

1. INTRODUCTION

Carbon nanotube field effect transistors (CNFET) have increasing potential to replace the conventional MOSFETs and hence, increasing demand to be the root of future integrated circuits. This is due to CNFET's reduced short-channel effects, good electrical conduction [1], large on current [2] and low fabrication cost compared to the silicon based MOSFETs. Also, the 10-fold increase [3] of the worldwide production of carbon nanotube (CNT) over the past decade

[1]*correspondin author*

2010 *Mathematics Subject Classification.* 94C99.

Key words and phrases. CNFET; fast adder; switching power; dynamic power; Cadence.

reflects the huge interest in the commercial market. However, researchers got increasingly attracted on CNFETs because of its capability of device performance variation by using various physical phenomenon within the channel [4] and also, by varying the threshold voltage through the CNT diameter variation (1-3 nm) [5].

In the literature, many brilliant designs of full adder circuits are found, some of which shows faster speeds and some shows lower power consumptions. An adder using 28 transistors has been implemented using conventional CMOS in [6]; although it has a low power consumption, it uses larger area and hence, becomes costly. The design with Transmission Gate Adder of 20 transistors [5] has the advantage of lower power consumption and less cost. High speed performance can be possible if CNFETs are used in the design for which less transistor count and less stages are required. Such design examples include full adder design using 14 transistors and 3 capacitors [7] and using 12 transistors and 3 capacitors [8] based on majority-not function. Full adder circuits with less number of transistors can be implemented using pass transistor logic. This design has the merits of reduced power consumption [9-11], lower chip area, less voltage supply [12] and less delay [13].

In this work, a six-transistor (6T) pass transistor logic based full adder module using CNFET has been designed and implemented using Cadence tool suite. So far seen in the literature, there are no works which particularly determine the switching power, although there are a number of research works which are related with the determination of total power consumed. Therefore, the aim of this work is to determine the switching power as well as to investigate its physical insight. The MOSFET-like CNFET has planar gate structure and uses zigzag single-walled CNT material of chirality (19, 0). In order to implement the CNFET in Cadence the Stanford CNFET Verilog-A model [14] has been used. 32 nm process technology has been chosen to match with the current trend of conventional Si-based process.

2. Preliminaries

2.1. **Structure of Fast Adder.** The proposed full adder using CNFET is shown schematically in Fig. 1.

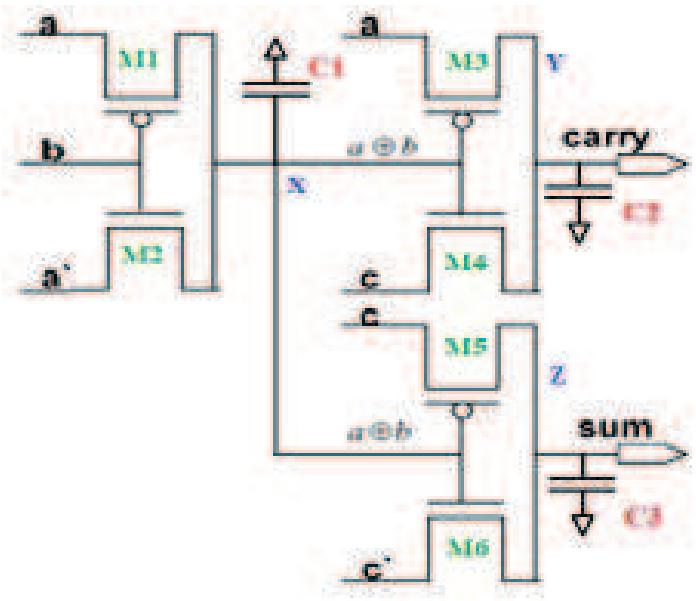

FIGURE 1. 6T Full Adder circuit implemented using CNFET. C1, C2, C3 are capacitances formed at various nodes.

A basic full adder cell has three 1-bit inputs 'a', 'b' and 'c' and two 1-bit outputs known as 'sum' and 'carry'. The logical Boolean expressions using truth table between the logic inputs and logic outputs based on 'Exclusive OR' logic can be expressed as:

$$sum = \overline{(a \oplus b)c} + (a \oplus b)\overline{c}$$
$$carry = \overline{(a \oplus b)}a + (a \oplus b)c$$

Where Exclusive–OR shown by '$\oplus$ ' performs the following Boolean Function-

$$(a \oplus b) = \overline{a}b + \overline{b}a$$

In this design '$(a \oplus b)$' signal is passed through the pass transistor multiplexer of the first stage made of two transistors (T1, T2) In the second stage, '$(a \oplus b)$' signal is sent to the bottom multiplexer (made of T3, T4) to choose between '$\overline{c}$ ' and 'c' to generate 'sum' and is sent the top multiplexer (made of T5, T6) to choose between 'a' and 'c' to generate 'carry'.

2.2. **Switching Power.** Switching power is occurred when a FET is switching its state and is due to the non-ideality of MOSFET. Also known as dynamic power, this power is the sum of transient power consumption $(P_{transient})$ and

capacitive load power (P_{cap}) consumption. $P_{transient}$ represents the amount of power consumed when the device changes logic states, i.e. "0" bit to "1" bit or vice versa. The necessary power to charge the load capacitance is called capacitive load power consumption. Therefore, the switching power can be expressed as [15]:

$$P_{switching} = P_{cap} + P_{transient} = (C_L + C)Vdd^2fN^3, \tag{2.1}$$

where C_L is the load capacitance, C is the internal capacitance of the CNFETs, f is the frequency of operation and N is the number of bits that are switching. Equation (2.1) reveals that as performance increases the speed and frequency of the IC increases and hence, the amount of switching power also increases. From equation (2.1), it is also observed that the switching power is data dependent and is, in fact, closely tied to the number of transistors that change states.

2.3. **Implementation in Cadence.** For the implementation of 1 bit 6T full adder circuit using CNFET in Cadence, the CNFET model library was imported from Stanford CNFET model [14] in Virtuoso Platform in cadence. Both P-type CNFET and N-type CNFET has three level named as Bottom , Mid and Top level having a (.va) extension. All these three level have five basic ports of FET. For the parameters of the CNFET model a (.vams) file was created. For FET implementation 32 nm process technology has been chosen. The library was created in virtuoso and then a symbol for the model was created. Afterwards the created symbol has been used to implement a fast adder circuit for simulation in the 'Schematic XL'. The simulation is done using 'Spectre' simulator. For transient analysis the 'Analog Design Environment L' is used. Fig. 2 shows the fast adder circuit implementation using CNFET in Cadence and the various parameters of the CNFET are tabulated in Table I. This section presents and discusses the results obtained using the simulations of 32 nm CNFET Verilog-a model [14] based 1 bit fast adder circuit using the Cadence tool suite. The fast adder circuit uses a 0.9 V as logic '1' and 0 V as logic '0' and digital inputs of 25, 50 and 100 MHz frequency. As load, a 2f F capacitive load is considered. The simulation results are presented and analyzed for the 'sum' and 'carry' outputs of the fast adder circuit. Fig. 3 shows the timing diagrams of 'sum' outputs of the 6T CNFET based fast adder circuit. From this figure, it has been observed that there is no output degradation for four input states, for the remaining four input states,

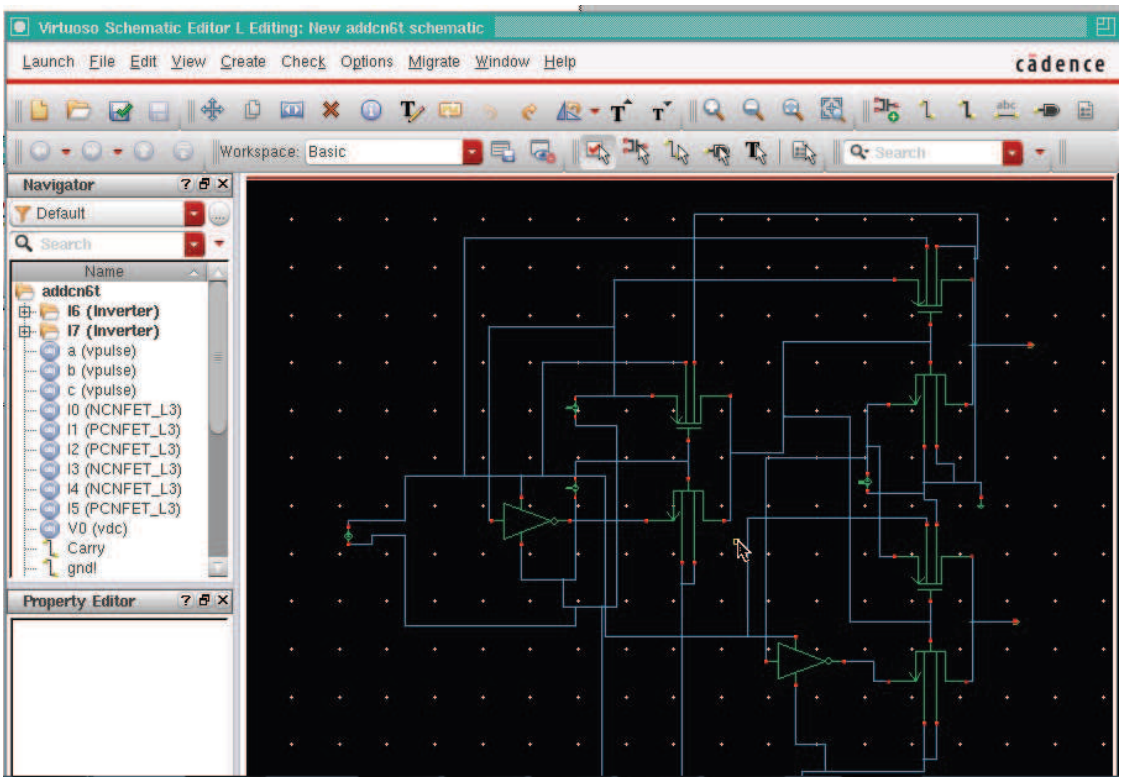

FIGURE 2. Fast adder circuit using cadence in schematic editor.

TABLE 1. Simulation Parameters

CNFET Model	MOSFET-like-CNFET
Number of Tubes	1
Module	1 Bit Fast Adder
Transistor Count	6
Corrupted Result	None
Temperature	27^0C (300K)
I_{on}	36.1366uA
I_{off}	131.4683pA

the output has been degraded. The output degradation is caused whether an NMOS passes a logic '1' and a PMOS passes a logic '0', since an NMOS is a poor conductor for logic '1' and a good conductor for logic '0', whereas, a PMOS is a good conductor for logic '1' and a poor conductor for logic '0'. Table I lists

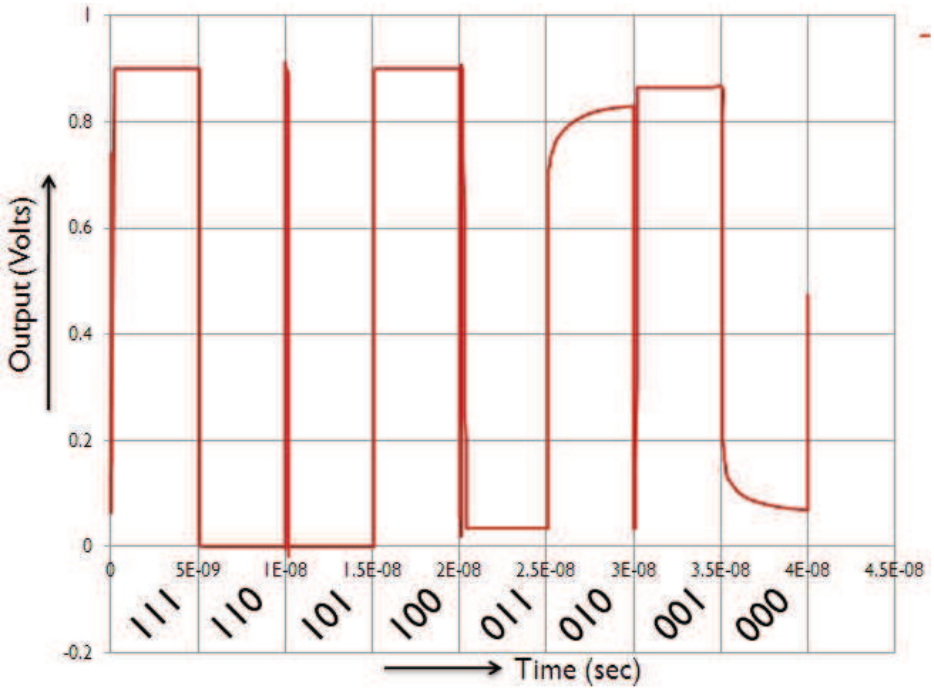

FIGURE 3. Voltage vs. time of 6T Full Adder 'sum' output with 2fF load.

TABLE 2. Simulation Parameters

cba	a ⊕ b	States of M6, M5	Logic Level Passed	Output level of 'sum'
111	0	OFF, ON	c =1	Strong 1
110	1	ON, OFF	c`=0	Strong 0
101	1	ON, OFF	c`=0	Strong 0
100	0	OFF, ON	c=1	Strong 1
011	0	OFF, ON	c=0	Weak 0
010	1	ON, OFF	c`=1	Weak 1
001	1	ON, OFF	c`=1	Weak 1
000	0	OFF, ON	c =0	Weak 0

the output levels of 'sum' for various digital input combinations. It has been revealed that the output levels listed in Table II are in well agreement with those shown in Fig. 3. Fig. 4 Shows the timing diagrams and Table III lists the output levels of 'carry' of the 6T CNFET based fast adder circuit. Again the output degradations for the digital input combinations of '110', '101', '100' and '000'

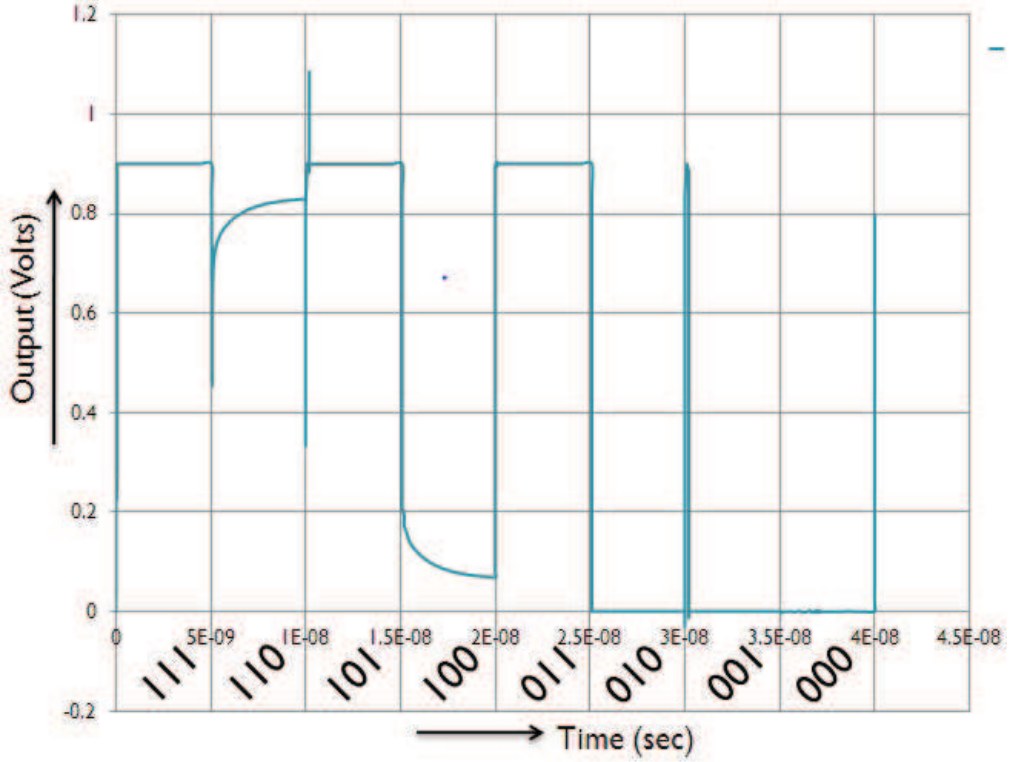

FIGURE 4. Voltage vs. time figure of 6T Full Adder 'carry' output with 2f F load.

observed in Fig. 4 are in well agreement with the corresponding listed levels in Table III. From the 'carry' output it is seen that there is output degradation for 100 and 110 input states. This is because of the fact that for these two states first stage of the circuit gets degraded output and also, in the second stage (carry branch) NMOS turns on and PMOS cannot be fully turned off [16]. All the carry and sum outputs are obtained in 0.9 V logic level voltage and this is very low voltage for the GDI (gate diffusion input) based circuit. So 'carry' and 'sum' outputs of the CNFET based adder are better than any other GDI based fast adder circuit. In the 6T 1 bit FA circuit, three capacitances, namely C1, C2 and C3 are formed at node X, Y and Z respectively as shown in Fig.1. C1 at X node contains the drain capacitances of M1 and M2 and the gate capacitances of M3, M4, M5 and M6, whereas, C2 at Y node and C3 at Z node contain only the drain capacitances of M3 and M4 and the same of M5 and M6 respectively. Hence, C1 must be greater than both C2 and C3. Fig. 5 shows how capacitances are formed

TABLE 3. Output logics at 'carry'

cba	a ⊕ b	States of M4, M3	Logic Level Passed	Output level of 'carry'
111	0	OFF, ON	A=1	Strong 1
110	1	ON, OFF	C=1	Weak 1
101	1	ON, OFF	C=1	Weak 1
100	0	OFF, ON	A=0	Weak 0
011	0	OFF, ON	A=1	Strong 1
010	1	ON, OFF	C=0	Strong 0
001	1	ON, OFF	C=0	Strong 0
000	0	OFF, ON	A=0	Weak 0

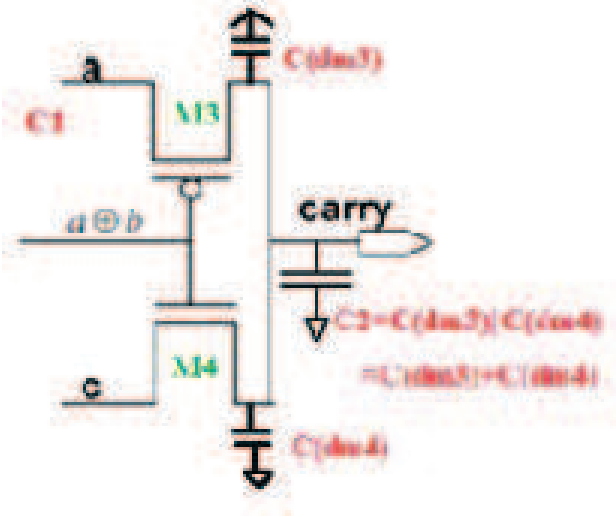

FIGURE 5. 6T Full Adder circuit's carry network capacitance formation and calculation

and calculated in a 6T Full Adder circuit's carry network. From this figure, it is seen that C(dm4) and C(dm3) is the combinations of several capacitances, such as drain-to-body, drain-to-gate, drain-to-channel, channel-to-substrate etc. C(dm4) and C(dm3) varies due to the change of combinations for various states. The same logic holds for 'sum' circuit. For the calculation of effective capacitance and its variation with respect to various input states 'captab' tool in cadence is used. Fig. 6 plots the variations of all the three capacitances against the state variations. From this figure, it has been observed that when a transistor turns 'ON' strongly and passes the strong signal, the output node for that transistor

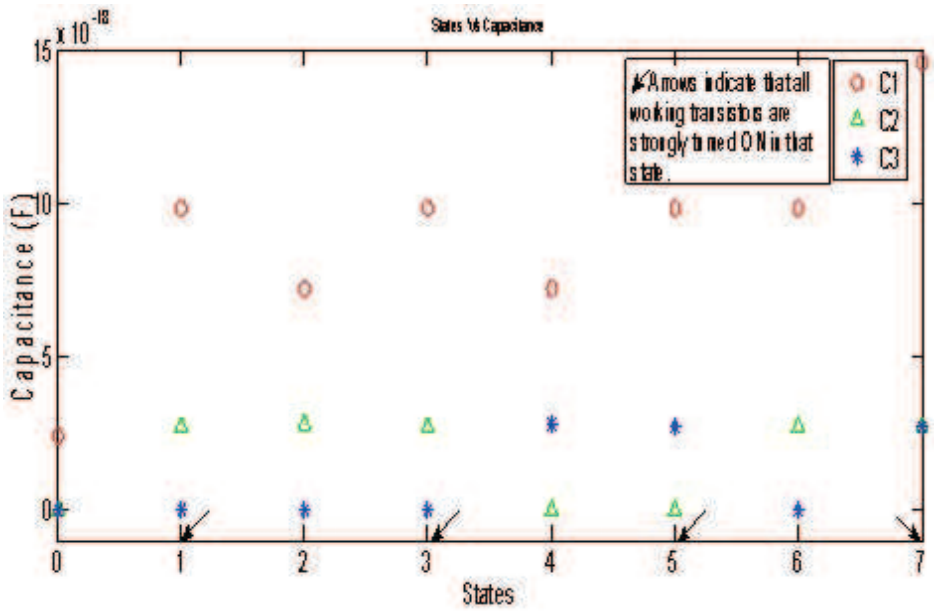

FIGURE 6. Variation of Capacitances (C1, C2, C3) with state variation

sees the maximum capacitance for that particular node and vice versa. This figure also agrees with the fact that C1 > C2, C3, as mentioned earlier. Therefore, in the 6T 1 bit FA, PSWITCHING must be dominated by C1 and follows closely the variation of C1 against the input variations. Fig. 7 Shows the switching power of 6T CNFET fast adder circuit for different input states. From this figure it is generally observed that the switching power is high when the input majority bits are '1' and is low when majority bits are '0'. The output capacitance is considered as '1' (High) when majority input bits are '1' and vice versa [17]. As the majority bits are '1' , the effective capacitance increases for the input states of '011', '101', '110' and '111'. So the switching power dissipation is high for these states. It is also observed that for the input states of '001' the switching power is also high. Indeed, for this input 'sum' switches High to Low and 'carry' switches low to High. A close observation of Fig. 6 and Fig. 7 reveals a close match of the variations of the capacitance and the switching power against the state variations, as expected.

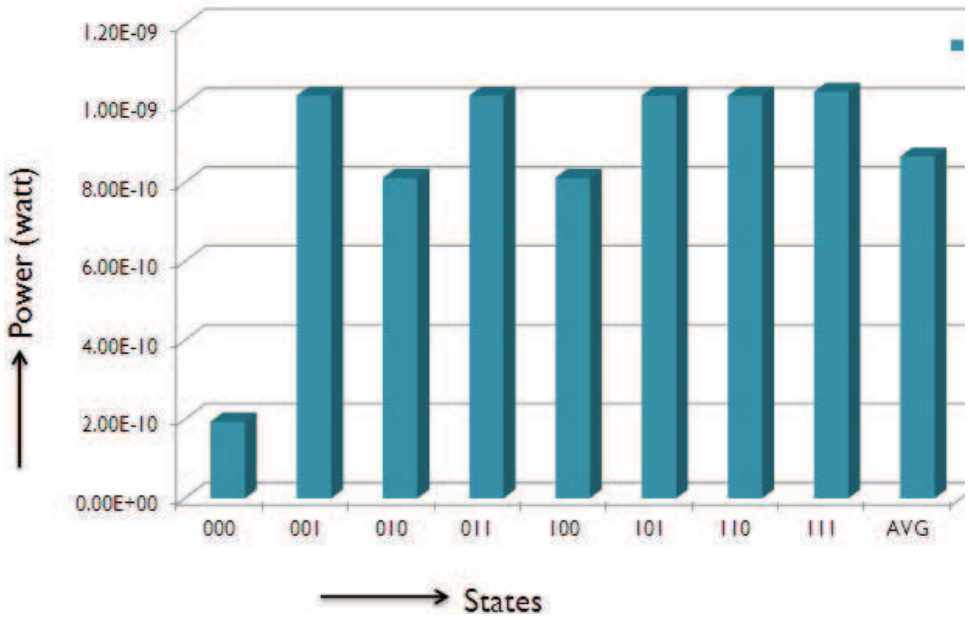

FIGURE 7. Switching Power vs. states without load

3. CONCLUSION

This paper presents an investigative analysis of switching power for different state variations for a pass transistor logic based fast adder module. The module uses CNFET transistors and has been implemented in Cadence. The simulation results show that the switching power of the implemented module varies in the same way as the capacitance seen at the output of the first stage of the module varies and that the outputs have degradation for one/two states. Therefore, a better physical insight of the switching power can be obtained through this work

REFERENCES

[1] T. RAVI, V. KANNAN: *Modelling and performance analysis of ballistic carbon nanotube field effect transistor (CNFET)*, International Conference on Recent Advances in Space Technology Services and Climate Change, RSTS and CC, 2010, 327–331.

[2] B. LIU, Z. CAO, J. TAO, X. ZENG, P. TANG, P. H-S. WONG: *Intel LVS Logic as a Combinational Logic Paradigm in CNT Technology*, IEEE International Symposium on Nanoscale Architectures, 2010.

[3] M. F. L. DE VOLDER, S. H. TAWFICK, R. H. BAUGHMAN: *A. John Hart, Carbon Nanotubes: Present and Future Commercial Applications*, Science, **339** (2013), 535–539.

[4] T. J. KAZMIERSKI, D. ZHOU, B. M. AL-HASHIMI: *HSPICE implementation of a numerically efficient model of CNT transistor*, Forum on Specification and Design Languages, (FDL), 2009, 1–5.

[5] B. EBRAHIMI, A. AFZALI-KUS: *Realistic CNFET based SRAM cell design for better write stability*, 1st Asia Symposium on Quality Electronic Design (ASQED), 2009, 14–18.

[6] C. H. CHANG, J. GU, M. ZHANG:*A review of 0.18-/spl mu/m full adder performances for tree structured arithmetic circuits*, IEEE Trans.Very Large Scale Integr. (VLSI) Syst., **13**(6) (2005), 686–695.

[7] A. KHATIR, S. ABDOLAHZADEGAN, I. MAHMOUDI: *High speed multiple valued logic full adder using carbon nano tube field effect transistor*, 2011.

[8] M. R. RESHADINEZHAD, M. H. MOAIYERI, N. KAIVAN:*An Energy-Efficient Full Adder Cell Using CNFET Technology* , IEICE Transactions on Electronics, **95** (2012), 744–751.

[9] H. T. BUI, Y. WANG, Y. JIANG: *Design and analysis of low-power 10-transistor full adders using XOR XNOR gates*, IEEE Trans. Circuits Syst. II, Analog and Digi-tal Signal Processing, **49**(1) (2002), 25–30.

[10] J. F. LIN, Y. T. HWANG, M. H. SHEU, C. C. HO: *A novel high speed and energy efficient 10- transistor full adder design*, IEEE Trans. Circuits Syst. I, **54**(5) (2007), 1050–1059.

[11] Y. JIANG, A. AL-SHERAIDAH, Y. WANG, E. SHA, J. G. CHUNG: *A novel multiplexer-based low-power full adder*, IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, **51** (2004), 345–348.

[12] S. GOEL, A. KUMAR, M. BAYOUMI: *Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style*, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., **14**(12) (2006), 1309–1320.

[13] M-B. LIN: *Introduction to VLSI systems A logic, circuit and system perspective*, Taylor and Fransis group, ch. 7, 2013.

[14] https://nano.stanford.edu/stanford-cnfet-model.

[15] N. E. WESTE: *CMOS VLSI Design: A Circuits and Systems Perspective*, Boston: Addison-Wesley, 2010.

[16] W. AL-ASSADI : *Pass-transistor logic design*, International Journal of Electronics Theoretical and Experimental, **70**(4) (1991), 739–749.

[17] H. R. NAGHIZADEH: *Design of Two High Permormance 1-Bit CMOS Full Adder Cells*, International Journal of Computing and Digital Systems, **2**(1) (2013), 47–52.

Department of Electrical and Electronics Engineering
United International University
Badda, Dhaka, Bangladesh
E-mail address: zubair@eee.uiu.ac.bd

Department of Electrical and Electronics Engineering
United International University
Badda, Dhaka, Bangladesh
E-mail address: provat335@gmail.com

Department of Electrical and Electronics Engineering
United International University
Badda, Dhaka, Bangladesh
E-mail address: taima.nabila@yahoo.com

Department of Electrical and Electronics Engineering
United International University
Badda, Dhaka, Bangladesh
E-mail address: epsi91@hotmail.com

Department of Electrical and Electronics Engineering
United International University
Badda, Dhaka, Bangladesh
E-mail address: ibchy@eee.uiu.ac.bd